

EMBEDDED DAB DECODER IP FOR 3G/4G MOBILE APPLICATION

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Abstract

This paper reports a DAB (Digital Audio Broadcasting) receiver decoder IP with extremely low power dissipation and low gate count. The IP structure, the evaluation kit, and the IC design are covered. The work embedding the IP within the ARM926 processor is described in details. The innovative IP enables DAB function to be embedded into 3G/4G baseband chip at very low cost.

Key words

DAB Decoder; DAB IP; 3G; 4G; baseband; SOC; ARM processor

Introduction

Until now, analogue radio signals have been subject to numerous types of interference. DAB can provide CD-like quality radio services even in a high speed vehicle. Aside from distortion-free reception and CD quality sound, DAB offers further advantages as it has been designed for the multimedia age to transmit text, pictures, data and even videos. For this reason, DAB is also called DMB (Digital Multimedia Broadcasting).

DAB/DMB combined with 3G/4G will benefit both sectors, including^{[1][2][3][4]}:

- The availability of one-to-many broadcasts enabling mobile operators to provide generic information to large group users.
- The development of low-cost, interactive entertainment services.
- The provision of reliable, constantly-updated information such as news alerts and other time sensitive services.

- The delivery of High Speed Downlink Packet Access (HSDPA) to mobile users, up to 1.5Mbps, more than the realistic estimates for 3G networks.
- The delivery of mobile phone TV program and interactive TV services.
- The merits of combining DAB Digital Radio's 'push' technology with mobile telephone's 'pull'.
- The opportunity to exploit the 'push/pull' combination by offering consumers continuous updates services on a low-cost monthly subscription basis, for example.

However, current DAB receiver solutions are still too expensive, too slow to decode video, and too power hungry to receive T-DMB on mobile handsets^{[5][6][7]}.

We have developed an efficient DAB decoder IP with extremely low power dissipation and low gate count. This IP can be integrated with a mobile baseband processor onto a single chip SOC. The work has been done to make the DAB IP a peripheral module of an ARM core so mobile handset designers can easily operate DAB/DMB decoder under the control of an ARM processor.

This paper introduces the design of DAB decoder IP and DAB receiver demo kit as well as field test results. The incorporation of DAB with ARM processor is also covered.

DAB IP design

The DAB decoder IP is a low power, minimum silicon implementation of a DAB receiver baseband decoder and MPEG L2 audio decoder, aimed for portable applications. The block diagram is shown in Figure 1.

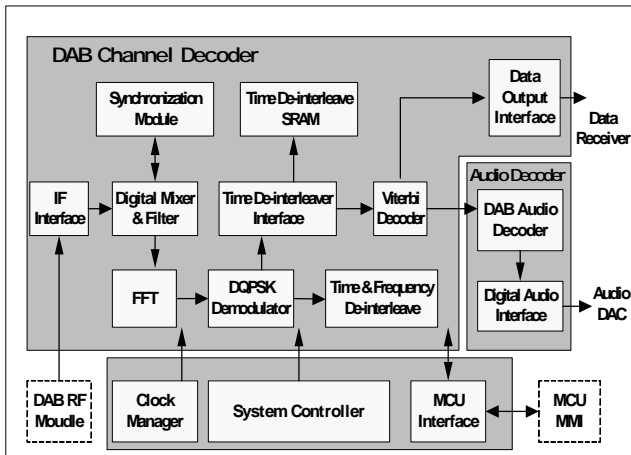


Figure 1: Block diagram of DAB decoder IP

The DAB IP design is technology independent, providing digital mixing, synchronization/tracking and demodulation of a full rate DAB ETSI 300 401 ensemble. It receives the DAB IF signal at 38.912MHz and can concurrently demodulate 2 sub-channels of audio, data & video in a single ensemble, making audio available via the on-chip MPEG L2 audio decoder, and making data & video available to a host processor for video/data decoder and display. The combination of this highly compact design and the high data rates provided by the DAB standard allow cost sensitive portable devices to receive multi-cast data at rates up to 1.5Mbps.

The baseband decoder comprises a digital mixer, a decimation filter, and a DAB channel (COFDM) decoder. The local frequency of the digital mixer is controlled by a synchronization module to best achieve frequency tracking/window alignment. A decimation filter with a sharp transition band effectively eliminates adjacent channel interference. The channel decoder consists of FFT, DQPSK, Frequency/Time De-interleave and Viterbi decoder.

The size of the time de-interleave SRAM may be selected according to the decoding rate required. A 64Kbyte SRAM is required for decoding rates up to 384Kbit/s, or 256Kbyte allows up to full rate. Two sub channels (up to four sub channels) can be decoded concurrently in one single DAB ensemble.

A user selected audio sub-channel is linked to the MPEG L2 audio decoder. The audio decoder complies with all features of the DAB MPEG audio decoder standard, including LSF (lower sampling frequency) mode. A mute function is activated automatically when the CRC detector indicates error.

The Digital Audio interface converts the decoded audio stream into a serial data format of Audio DAC, 16bit or 24bit, and applies DRC (dynamic range control). User selected video & data are available at the MMI & data receiver interface.

The design achieves a maximally compact IC architecture. Three proprietary multi-instruction DSP engines execute most of the functions, and all hardware resources are used with maximum efficiency. The design uses multi-clock domains to save power consumption. The highest clock frequency is only 65.536MHz.

The design achieves full DAB channel decoding capacity. When lower capacity channels are selected, most blocks are automatically switched to a sleep mode during unwanted symbols, including digital mixer, filter, FFT, DQPSK, and Viterbi decoder.

DAB IP evaluation Kit

A DAB IP evaluation kit has been designed. The evaluation kit is in fact a DAB receiver. The core of the receiver is the DAB decoder IP RTL design which was programmed onto an Altera Stratix FPGA device, EP1S10. Other devices include a RF module of DAB, an ADC, a MCU and an Audio DAC with amplifier. The block diagram of the evaluation kit is shown in Figure 2.

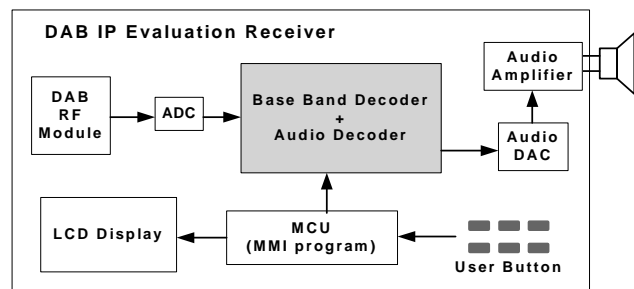


Figure 2: DAB IP evaluation kit

The evaluation kit works well in any area where DAB signal is available. Field tests have been carried out in many places including Guangdong and Beijing, China and London, M4 & M40 motorway, Southeast of England. All RF channels and sub-channel programs can be received with CD like quality even in high-speed vehicles.

IC design and fabrication

An IC design has been carried out to implement the DAB decoder IP into silicon. A 0.18 micron CMOS technology has been chosen and the design has been completed. Figure 3 shows the layout.

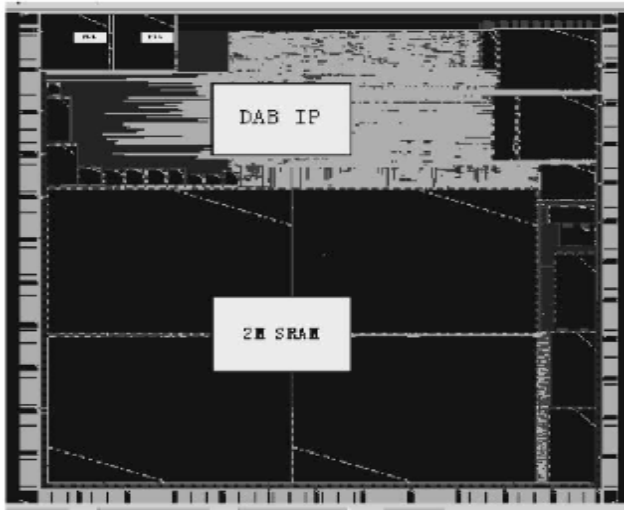


Figure 3: Layout of DAB IP in 0.18 micron CMOS technology

The total area for logic plus 400Kbit SRAM is only 5.0 mm^2 so it can be easily added on chip to a mobile baseband IC at very low extra cost. The calculated power dissipation is less than 50mW. The chip includes a 2Mbit SRAM for the time de-interleave function for a full rate DAB decoder, which occupies 12.8 mm^2 of silicon area. The total area of the chip is 21 mm^2 .

The chip is in fabrication and the test results will be fully reported in the conference.

Embedded DAB decoder IP into ARM based processor

With technical support from ARM, the DAB decoder

is embedded into an ARM926EJ-S board via AMBA (Advanced Microcontroller Bus Architecture)^{[8][9]}.

a. Treating DAB decoder as a peripheral module of ARM processor, and linking it to the AMBA peripheral bus (APB)

The DAB decoder has its own controller so it does not require ARM processor to manage internal decoding tasks. However, some user interface related tasks such as decoding FIC data, display and setting sub-channels are better to be done by the ARM CPU. The DAB decoder will send an interrupt signal to inform the CPU when FIC data are ready. The CPU then decides when and whether to decode the FIC data. Because FIC data are repeated program/service information etc, CPU response time to the interrupt is not critical. Therefore the DAB decoder can be treated as a peripheral module and linked easily to AMBA APB no matter how complicated the DAB decoding function is. In this case, the ARM CPU is the master and DAB decoder is the slave. The SPI (Serial Peripheral Interface) protocol can be used for their communication so ARM CPU can use a few wires to control the DAB decoder or download the data for the further processing. This way greatly reduces the complexity of embedding the DAB decoder into a mobile processor.

b. Sharing the time de-interleave SRAM with internal data SRAM of ARM processor

This is a significant step to further reduce the silicon area. From Fig 3 we see 2Mbit SRAM uses considerable silicon area. Therefore it is necessary to share the time de-interleave SRAM with other data SRAM in a mobile processor. Fortunately the ARM926EJ-S board provides open AMBA access and has a 8Mbit SRAM available via AMBA AHB (Advance High-Performance Bus) on the board. It is an ideal solution to use it to demonstrate such resource sharing. Figure 4 shows the DAB decoder IP embedded as a peripheral module to an ARM processor based on the single-layer AHB.

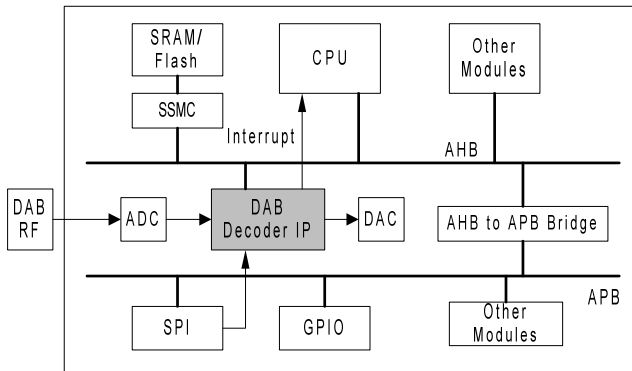


Figure4: The DAB decoder IP embedded into ARM processor based on single-layer AHB

But in this case, the DAB decoder is the master and it has to cooperate with the ARM CPU and the other master modules. The single AHB will be very busy with so many master accesses, so a better solution is required. The ARM926EJ-S board has a multi-layer bus working mode which is more configurable and efficient. The multi-layer AHB enables multiple bus masters to be active in parallel. Figure 5 shows the DAB decoder IP embedded as a peripheral module to an ARM processor based on multi-layer AHB.

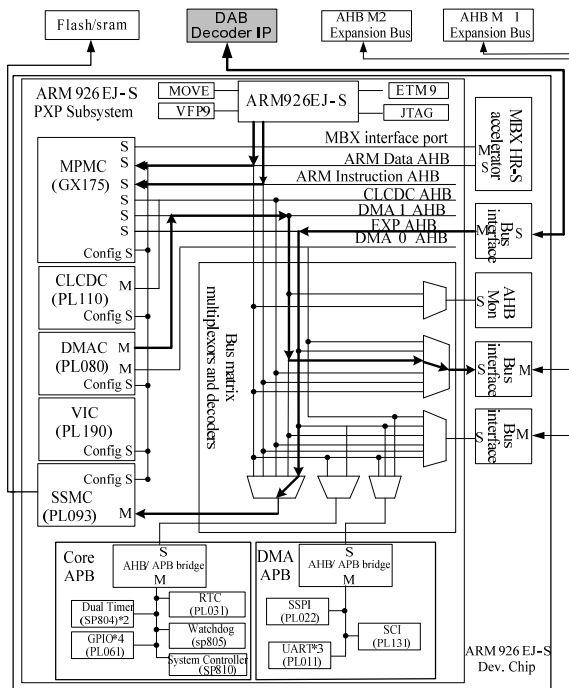


Figure5: The DAB decoder IP embedded into ARM processor based on multi-layer AHB

As Fig.5 shows, multiple masters can access buses simultaneously. The DAB decoder accesses SRAM through EXP-AHB while the ARM CPU accesses MPMC through DATA-AHB and Instruction-AHB. This bus architecture gives the DAB decoder a more comfortable environment to be embedded and greatly improves system performance.

c. Sharing ADC, audio DAC, PLL, OSC with other applications

The DAB decoder needs an 8-10bit resolution, 8MSPS ADC, and an Audio DAC with 16/24bit resolution. The DAB decoder uses two primary clock frequencies, 65.536MHz and 18.432MHz. As these modules and frequencies are commonly used by many mobile applications, they are easily shared with other functions.

The above works make it possible to reduce the extra silicon area of embedded DAB decoder down to 5.0 mm² for 0.18μm CMOS process.

Conclusion

Our innovative DAB baseband IP design can achieve significant improvement on power dissipation and cost reduction compared to the current market solutions. The very small silicon area required for the IP implementation means the DAB decoder can be integrated on chip with 3G/4G baseband chips. Embedding the DAB decoder IP within the ARM926 processor will benefit such designs.

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